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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,117	12/17/2001	Bernardo De Oliveira Kastrup Pereira	NL 000721	2411

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,117	DE OLIVEIRA KASTRUP PEREIRA ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 USC § 102(b) as being clearly anticipated by Abbott, U.S. Patent 6,006,321.

Abbott taught (e.g. see figs. 1-7b) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

A. a data processing device (fig. 7a) configured according to a device configuration (col. 5 lines 20-35) so as to be capable of executing a program comprising an instruction (col. 6 lines 10-11), the device comprising;

B. a configurable functional unit (fig. 1) for executing the instruction according to a configurable function (col. 3 lines 14-23) that is configured outside the instruction (col. 19 lines 29-52), the configurable functional unit including;

C. a unit input for (108) inputting a plurality of bits of one or more source registers (104, 106) specified by the instruction (col. 19 lines 63-66, because all operations in a CPU occur due to the execution of instructions, an instruction execution will have been the source of this specification), a unit output (120) for outputting a plurality of bits of a result to a destination register (104, 106) specified by the instruction (col. 19 lines 63-66);

D. a plurality of independent configurable logic blocks (fig. 7a, 702a ... 702;, fig. 7b, FPD 732a ... 732;) for performing programmable logic operations (col. 3 lines 6-22) to implement the configurable function and producing outputs having a first order of bits (inherent, any output of bits will have a first order, the natural order that the circuits produce the bits);

E. a first programmable connection circuit (fig. 2, 202) between the unit input (fig. 1,

108) and the logic blocks (fig. 2, 212), for selectively coupling inputs of the logic blocks to bits from the unit input, dependent on the configured function (col. 6 line 37 to col. 7 line 25);

F. a second programmable connection circuit (fig. 4, 410) between the logic blocks and the unit output (fig. 1, 120), for selectively coupling bits of the outputs of the logic blocks to the unit output in a second order of bits, dependent on the configured function (col. 12 line 1 to col. 13 line 43).

4. As to claims 2 and 3, Abbott taught each logic block having a plurality of outputs (fig. 2, 48 bits from 202, 48 bits from "SELECTIVE FIELD NEGATION CIRCUIT", 64 bits from "REDUCTION NETWORK BANK", and 64 bits from 214), at least one of the bits of the unit output being connectable exclusively to one of the outputs of each logic block (col. 12 lines 8-10 and 24-39), the second programmable connection circuit comprising a multiplexer (col. 12 lines 5-11) for coupling the one of the outputs of a selected one of the logic blocks to the at least one of the bits of the unit output.

5. As to claim 4, Abbott taught that either the first programmable connection circuit or the second programmable connection circuit having a fixed, unprogrammable connection to an input or output of one of the independent configurable logic blocks and a programmable connection to a remainder of the inputs and outputs (col. 6 line 64 to col. 7 line 25, wherein grouping bits into sets provides a "fixed unprogrammable connection" of that set of bits, i.e., the bits within the set can not each be independently connected).

6. As to claim 5, Abbott taught a method of programming a configurable processing device according to a device configuration to perform a processing task, wherein the device includes a configurable processing unit that includes one or more programmable logic blocks (see details, supra.) the method comprising;

A. identifying a special complex of operation that occurs in the task and requires one or more operand data words and produces a result data word (col. 19 lines 23-31, in order to configure the devices the CPU must have identified an operation suitable for the

device);

B. searching for an assignment of logic operations for producing different bits of the result data word to different ones of the programmable logic blocks, so that the logic operations for producing a subset of the bits of the result data word that, if implemented together in the programmable logic blocks, would exceed the capacity of that one of the programmable logic blocks, are distributed over different ones of the logic blocks (figs. 7a and 7b detail plural FPD devices in Abbott's embodiment. It would have been inherent that in order to fully utilize the plurality of FPD devices that operations must have been distributed across the plurality of logic blocks in a appropriate manner);

C. programming each of the programmable logic blocks to perform the logic operations for the bits of the result data word assigned to it (col. 19 lines 28-32 and 56-57);

D. programming connection circuits in from the programmable logic blocks and subsequent to the logic blocks so as to perform a first routing of bits of an operand of a special instruction to the programmable logic blocks that use those bits of the operand in the logic operations and so as to perform a second routing outputs of the programmable logic blocks to bits of the result data word to which the programmable logic blocks are assigned (col. 6 lines 54-63 and (col. 12 line 65 to col. 13 line 20).

7. As to claim 6, Abbott taught a method of executing a program with a processing device with a configurable function unit according to a device configuration (see details above), the method comprising

A. inputting one or more words of one or more operands of the configurable instruction into the configurable functional unit (fig. 1, 104, 106, 108), each word including a plurality of bits (fig. 2, 48 bits);

B. selectively coupling the bits of the words of the operands to inputs of logic blocks, dependent on a configured function (fig. 2, 202);

C. performing programmable logic operations to implement the configurable function to provide an output word that includes a plurality of bits (fig. 2, "SELECTIVE FIELD

NEGATION CIRCUIT", "REDUCTION NETWORK BANK");

D. selectively coupling bits of the output word to bits of a result word, dependent on a configured function (fig. 4, 410).

8. As to new claims 7-20, they do not teach or define above the invention claimed in claims 1-6 and are therefore rejected under Abbott for the same reasons set fourth in the rejection of claims 1-6, supra.

9. As to claim 11, Abbott taught that source registers of the one or more words from the plurality of registers were identified in an instruction that effects execution of a current function of the at least one configurable function unit (col. 6 lines 7-12, col. 1 lines 38-44, furthermore, it is inherent that instructions specify operands in modern computing systems).

10. As to claim 12, although Abbott did not specifically detail a destination register, it is inherent that all instructions contained an indication of a destination of the result of their requested computation.

11. As to claim 13, Abbott taught the instruction identifying the claimed source and destination registers as detailed above in the rejection of claims 11-12.

12. As to claim 18, Abbott taught an instruction issue unit that was configured to provide the instructions to the processor (col. 1 lines 38-39, in order for an "ADD" to be "issued" an "issue" unit must be present in the CPU).

13. As to claims 19 and 20, Abbott taught a configuration control circuit that was configured to provide the set of configuration data corresponding to the operand based on the configuration instruction from the issue unit (fig. 1, 110, 112, fig. 2, 112).

14. Applicant's arguments with respect to claims 1-6 have been considered but are deemed to be moot in view of the new grounds of rejection. As applicant failed to provide any arguments with respect to new claims 7-20, in clear violation of the requirements of MPEP § 714.04, there are no arguments to consider with respect to the new claims.

15. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02,

710.02(b)).

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
December 7, 2006

RICHARD L. ELLIS
PRIMARY EXAMINER